IN THE CLAIMS:

1. (Original) A low power operation control unit mounted in a microprocessor having an instruction condition executing function using a condition flag, the control unit controlling a low power operation of the microprocessor,

the control unit comprising a first instruction set including instruction execution control function information in a specific bit field of an instruction code inputted to a microprocessor, the information being used for selecting a flag for an instruction execution control function, and one or more second instruction sets including control specification information for low power control in the specific bit field,

wherein the control unit comprises:

an operation mode switching circuit for switching the instruction sets to execute the first instruction set during a normal operation and execute the second instruction set during a low power operation;

a predicate decision circuit for reading a flag corresponding to the instruction execution control function information in a

first instruction set mode to discriminate an instruction execution control operation;

a control specification information extraction circuit for extracting control specification information of a control circuit for reading the control specification information in a second instruction set mode and performing a low power operation; and

a controlling unit for performing a low power operation of each control circuit by using the control specification information,

wherein the instruction execution control function information and the control specification information are provided beforehand in each program for executing an instruction, and a low power operation of each control circuit is performed for each instruction according to the control specification information, thereby controlling a low power operation of the microprocessor for each instruction.

2. (Original) A low power operation control unit mounted in a microprocessor having an instruction condition executing function using a condition flag, the control unit controlling a low power operation of the microprocessor,

the control unit comprising a first instruction set including instruction execution control function information in a specific bit field of an instruction code inputted to a microprocessor, the information being used for selecting a flag for an instruction execution control function, and one or more second instruction sets including control specification information for low power control in the specific bit field,

wherein the control unit comprises:

an operation mode switching circuit for switching the instruction sets to execute the first instruction set during a normal operation and execute the second instruction set during a low power operation;

a predicate decision circuit for reading a flag corresponding to the instruction execution control function information in a first instruction set mode to discriminate an instruction execution control operation;

an event generating unit for reading the control specification information in a second instruction set mode and generating an event according to the control specification information; and

a controlling unit for performing a low power operation of each control circuit in response to the event,

wherein the instruction execution control function information and the control specification information are provided beforehand in each program for executing an instruction, and a low power operation of each control circuit is performed for each instruction according to the control specification information, thereby controlling a low power operation of the microprocessor for each instruction.

3. (Currently Amended) The low power operation control unit according to claim 1~~ or 2~~, wherein the control circuit is an operation stop deciding unit for deciding an operation stopping point on a specific point of a program, the controlling unit is an operation stop control unit for performing control to stop an operation on a given point of the microprocessor based on a decision result of the operation stop deciding unit, and a low

power operation of the microprocessor is controlled for each instruction by performing control to stop an operation on the given point of the microprocessor.

4. (Currently Amended) The low power operation control unit according to claim 1~~ or 2~~, wherein the control circuit is a power supply voltage deciding unit for deciding control on a power supply voltage on a specific point of a program, the controlling unit is a power supply voltage controlling unit for controlling a power supply voltage of the microprocessor based on a decision result of the power supply voltage deciding unit, and a low power operation of the microprocessor is controlled for each instruction by controlling a power supply voltage of the microprocessor.

5. (Currently Amended) The low power operation control unit according to claim 1~~ or 2~~, wherein the control circuit is a transistor body bias deciding unit for deciding control on a transistor body bias on a specific point of a program, the controlling unit is a transistor body bias controlling unit for controlling a transistor body bias of the microprocessor based on a

decision result of the transistor body bias deciding unit, and a low power operation of the microprocessor is controlled for each instruction by controlling a transistor body bias of the microprocessor.

6. (Currently Amended) The low power operation control unit according to claim 1 ~~or 2~~, wherein the control circuit is a clock frequency deciding unit for deciding control on a clock frequency on a specific point of a program, the controlling unit is a clock frequency controlling unit for performing control on a clock frequency based on a decision result of the clock frequency deciding unit, and a low power operation of the microprocessor is controlled for each instruction by controlling a clock frequency of the microprocessor.

7. (Original) The low power operation control unit according to claim 2, wherein one or more target microprocessors, each being a microprocessor other than the microprocessor comprising the event generating unit, or data processing units, comprise, as the controlling unit, an operation controlling unit for controlling a

low power operation of the microprocessor or the data processing unit, thereby controlling a low power controlling operation of the microprocessor or the data processing unit by the microprocessor comprising the event generating unit.

8. (Original) The low power operation control unit according to claim 2, wherein one or more target microprocessors, each being a microprocessor other than the microprocessor comprising the event generating unit, or data processing units, comprise, as the controlling unit, a power supply controlling unit for controlling a lower power controlling operation by controlling a power supply of the target microprocessor or the data processing unit, thereby controlling a low power controlling operation of the target microprocessor or data processing unit by the microprocessor comprising the event generating unit.

9. (Currently Amended) A program optimizing apparatus for the low power operation control unit according to claim 1~~—or—2~~, the apparatus being a microprocessor program optimizing apparatus generating the instruction code, the apparatus comprising:

a power consumption calculating unit for calculating a power consumption of operation stop control, power supply voltage control, transistor body bias control, or clock frequency control based on power consumption information of a microprocessor;

an operation control candidate calculating unit for calculating a power consumption of an operation control circuit candidate of each instruction by using the power consumption; and

a switching deciding unit for selecting an operation control circuit of each instruction to minimize the power consumption,

wherein the operation stop control is an operation stop control performed by the controlling unit on a given point of the microprocessor based on a decision result of an operation stop deciding unit, the power supply voltage control is a power supply voltage control performed by the controlling unit on the microprocessor based on a decision result of a power supply voltage deciding unit, the transistor body bias control is a transistor body bias control performed by the controlling unit on the microprocessor based on a decision result of a transistor body bias deciding unit, and the clock frequency control is a clock frequency

control performed by the controlling unit based on a decision result of a clock frequency deciding unit,

wherein an instruction set switching instruction for switching the first instruction set and the second instruction set is inserted, and the control specification information of the second instruction set is determined, thereby optimizing a program for performing a low power operation control is optimized.

10. (Original) A low power operation control unit mounted in a microprocessor having an instruction condition executing function using a condition flag, the control unit controlling a low power operation of the microprocessor,

the control unit comprising a first instruction set including instruction execution control function information in a specific bit field of an instruction code inputted to a microprocessor, the information being used for selecting a flag for an instruction execution control function, and one or more second instruction sets including control specification information for low power control in the specific bit field,

wherein the control unit comprises:

an operation mode switching circuit for switching the instruction sets to execute the first instruction set during a normal operation and execute the second instruction set during a low power operation;

a predicate decision circuit for reading a flag corresponding to the instruction execution control function information in a first instruction set mode to discriminate an instruction execution control operation;

a control specification information extraction circuit for reading the control specification information in a second instruction set mode and extracting control specification information of a control circuit for performing a low power operation;

a program throughput measuring unit for measuring a throughput on a specific point of a program by using the control specification information;

a throughput deciding unit for deciding an optimum power consumption for each program based on the throughput; and

a frequency/power supply controlling unit for controlling a frequency and a power supply voltage during program execution to have the optimum power consumption,

wherein a low power operation of the microprocessor is controlled for each instruction by measuring a throughput of a program corresponding to each instruction.

11. (Original) A low power operation control unit mounted in a microprocessor having an instruction condition executing function using a condition flag, the control unit controlling a low power operation of the microprocessor,

the control unit comprising a first instruction set including instruction execution control function information in a specific bit field of an instruction code inputted to a microprocessor, the information being used for selecting a flag for an instruction execution control function, and one or more second instruction sets including control specification information for low power control in the specific bit field,

wherein the control unit comprises:

an operation mode switching circuit for switching the instruction sets to execute the first instruction set during a normal operation and execute the second instruction set during a low power operation;

a predicate decision circuit for reading a flag corresponding to the instruction execution control function information in a first instruction set mode to discriminate an instruction execution control operation;

a control specification information extraction circuit for reading the control specification information in a second instruction set mode and extracting control specification information of a control circuit for performing a low power operation;

a program throughput measuring unit for measuring a throughput on a specific point of a program by using the control specification information; and

a throughput referring unit for making reference to the throughput as a variable in a program of the microprocessor,

wherein reference is made, during program execution, to a program throughput obtained for each instruction of a program operation.